

Fig. 1
(prior art)

100333-1444

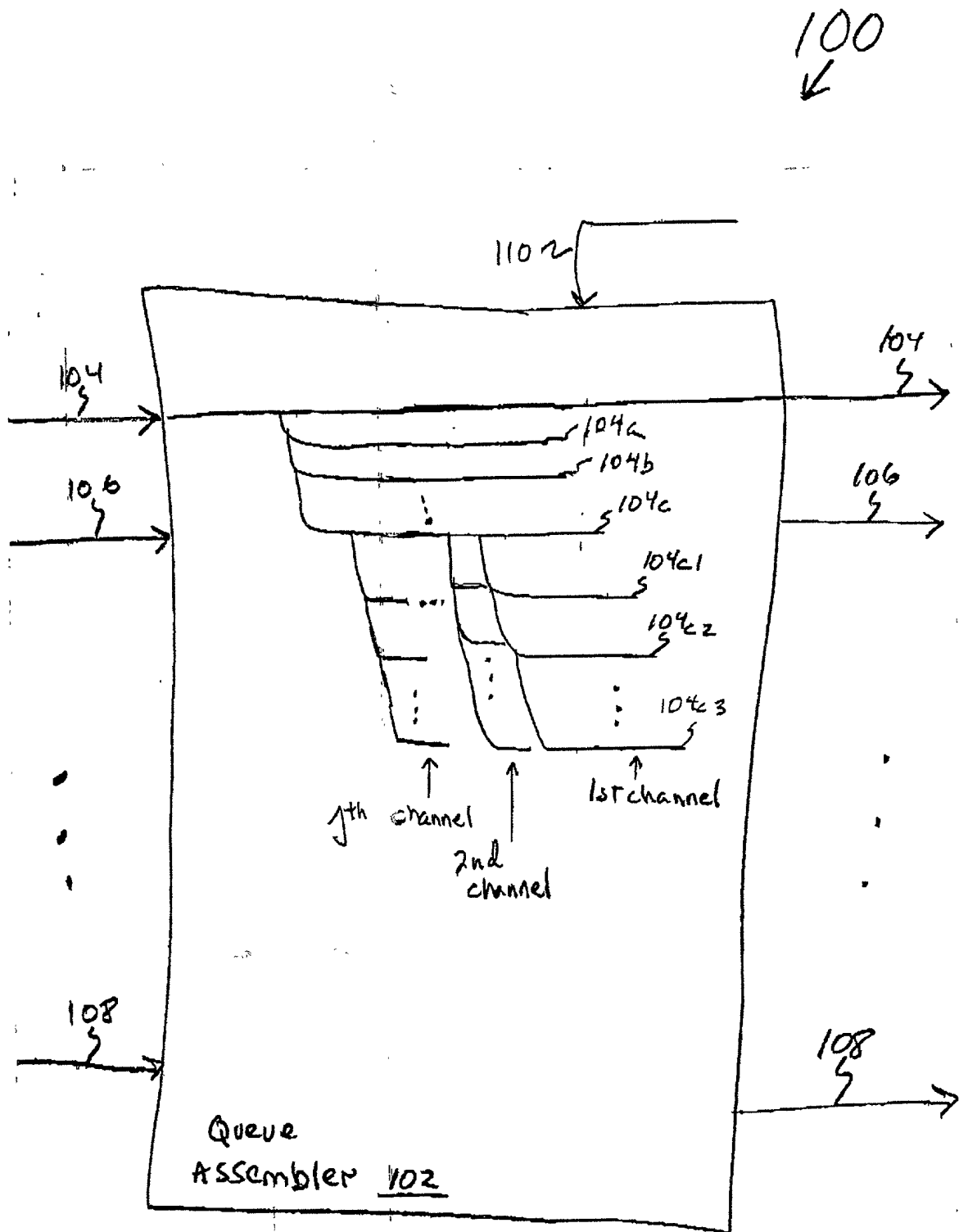


Fig. 2a

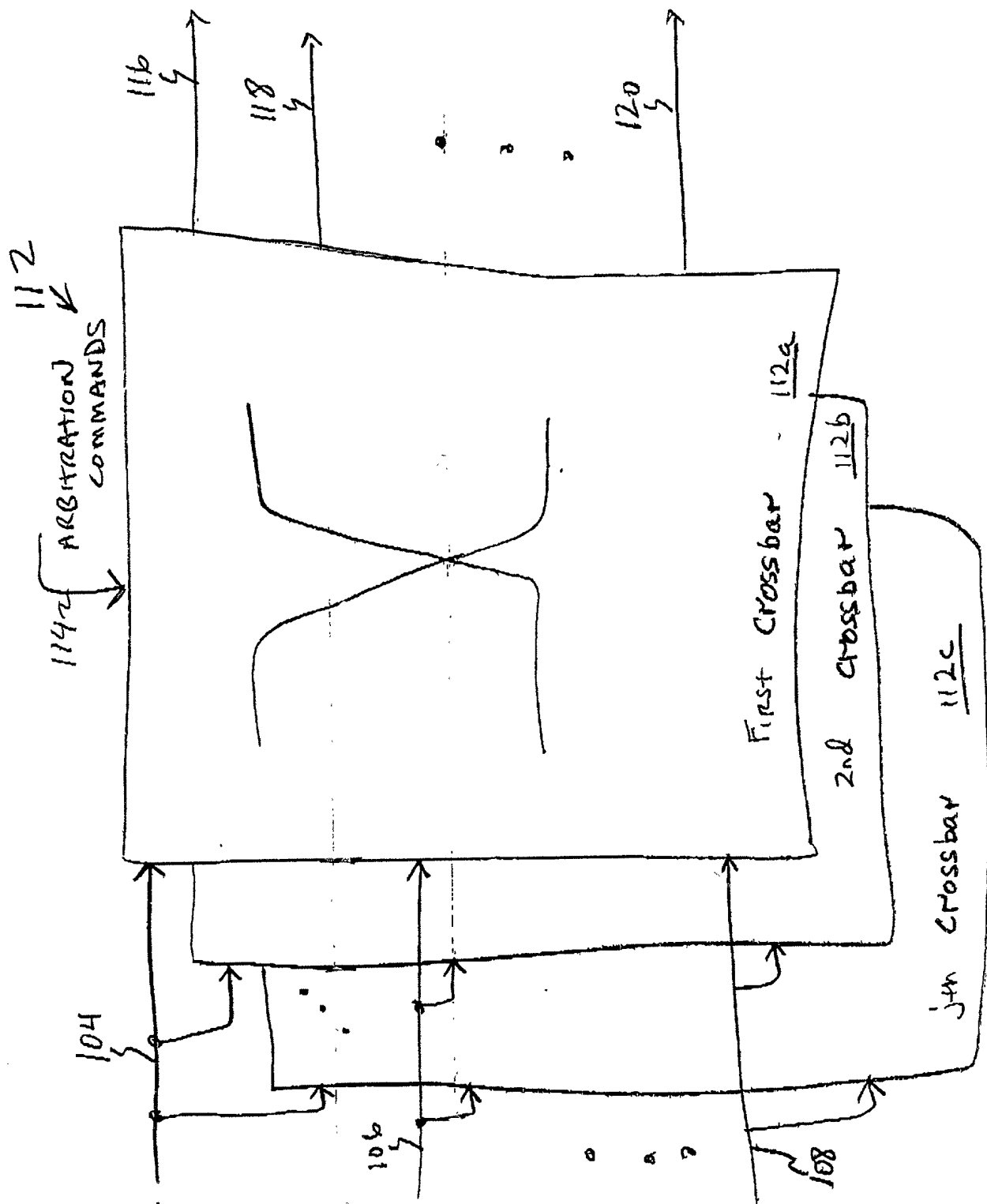


FIG. 26

100
114
132
134
136
142
144
150
160
162
164
174
180

100
114
132
134
136
142
144
150
160
162
164
174
180

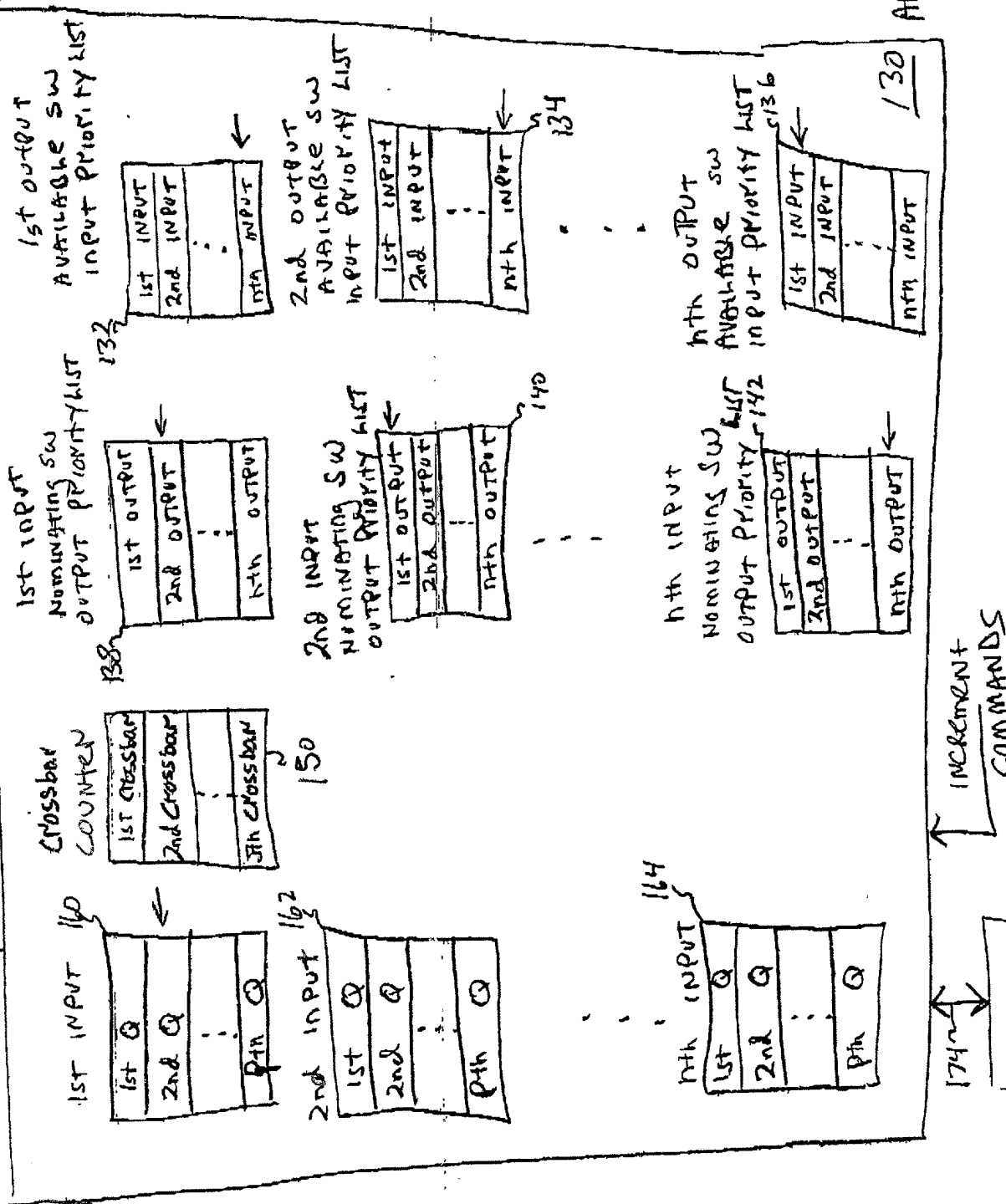
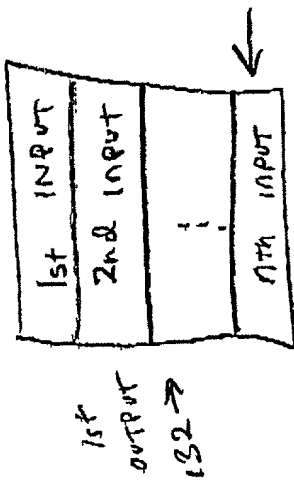


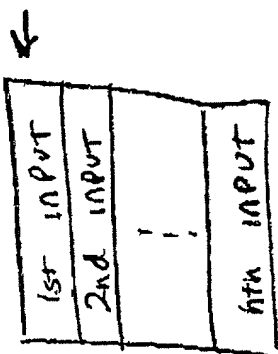
Fig. 3a

1ST ARBITRATION CYCLE

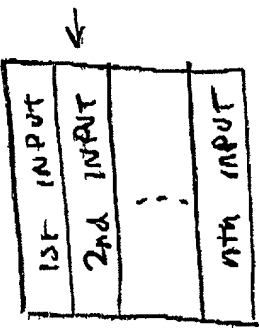
INITIAL STATE



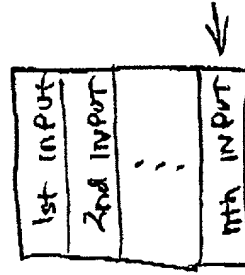
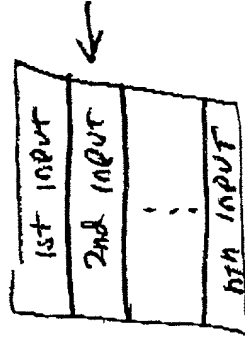
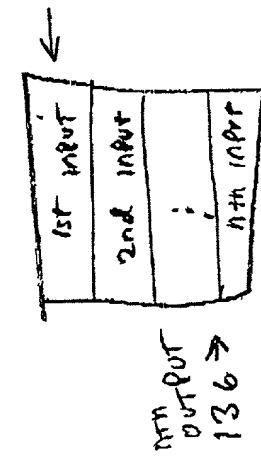
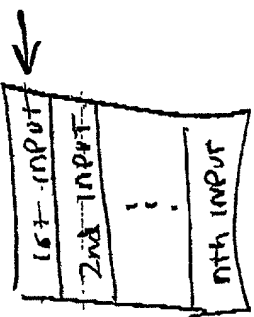
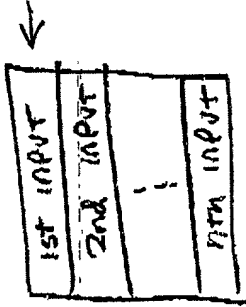
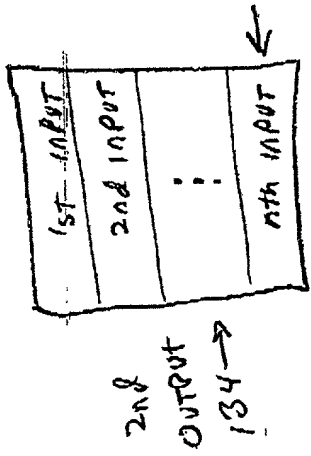
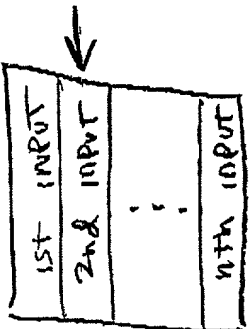
1st XBAR



2nd XBAR



jth XBAR



AVAILABLE SW INPUT PRIORITY LISTS

Fig. 3b

2nd ARBITRATION cycle

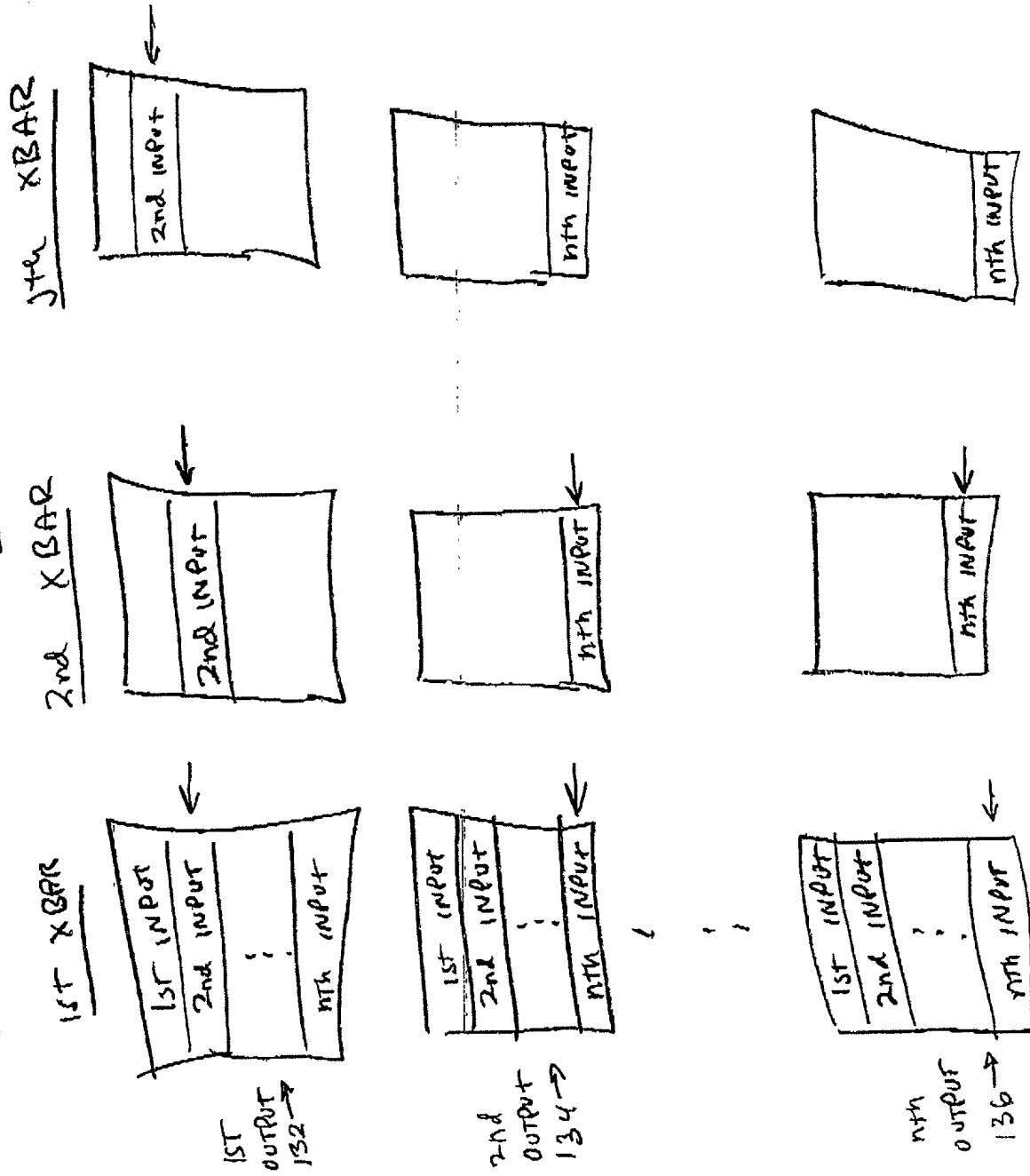


Fig. 3c

SW OUTPUT LUTS
1ST ARBITRATION CYCLE

NOMINATING
INITIAL STATE

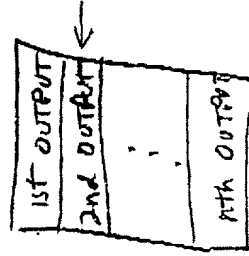
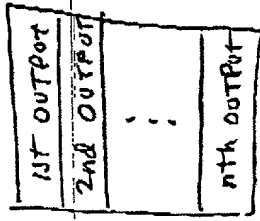
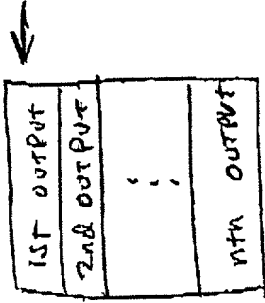
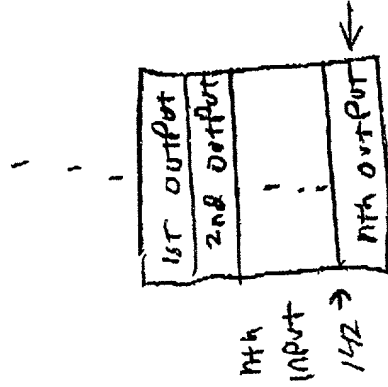
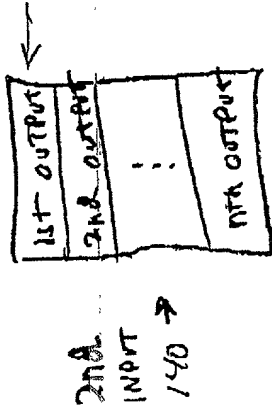
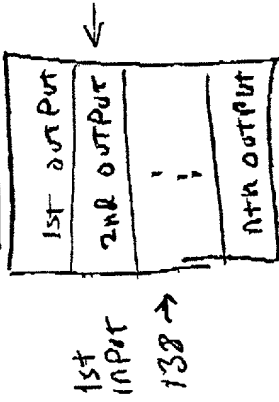
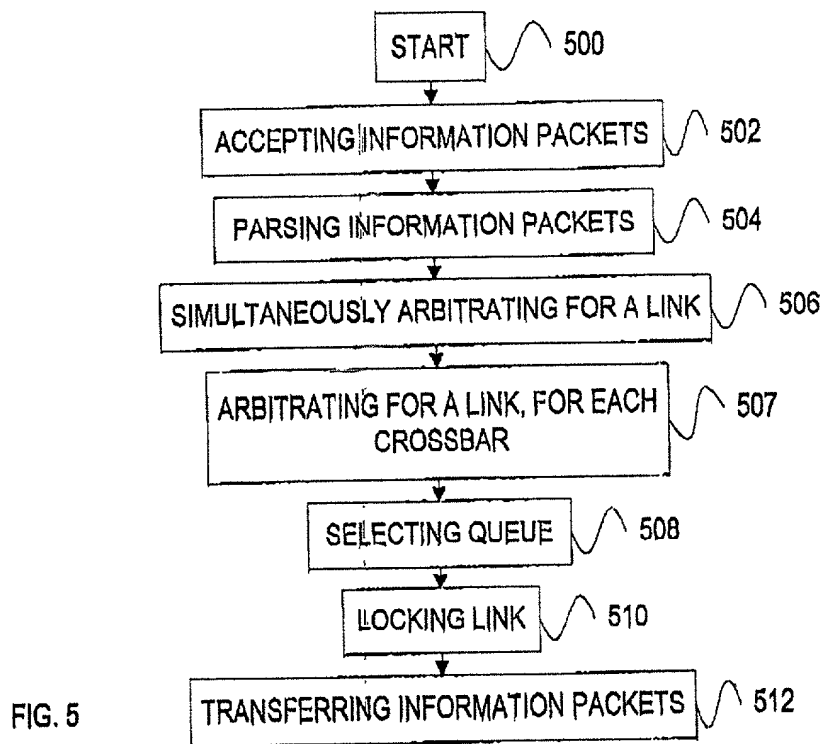
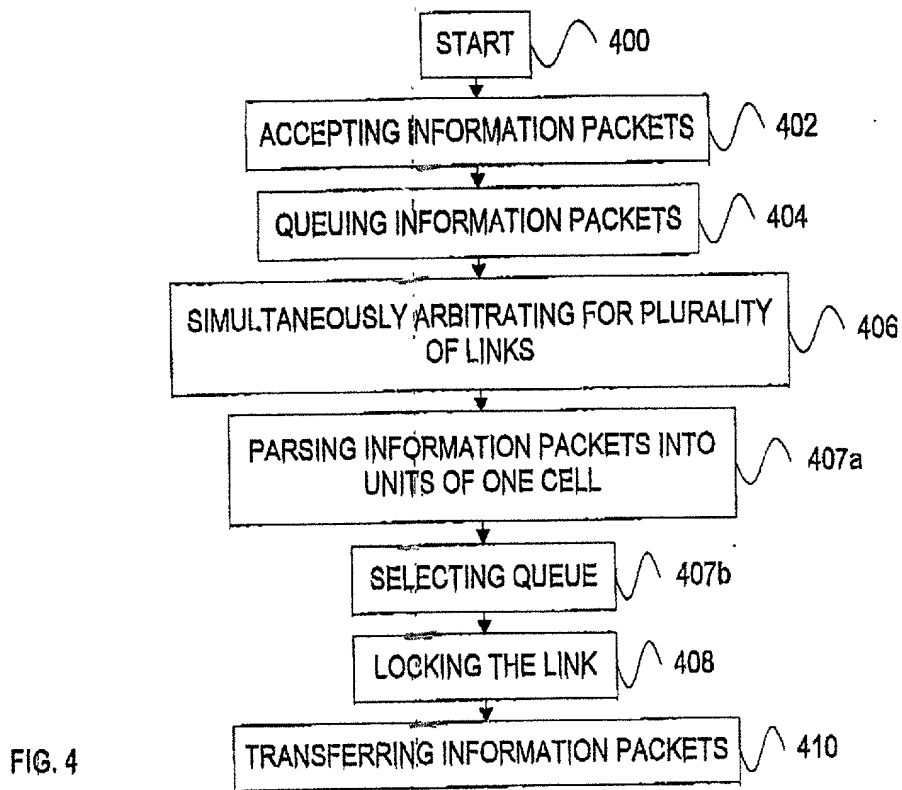


Fig. 3d



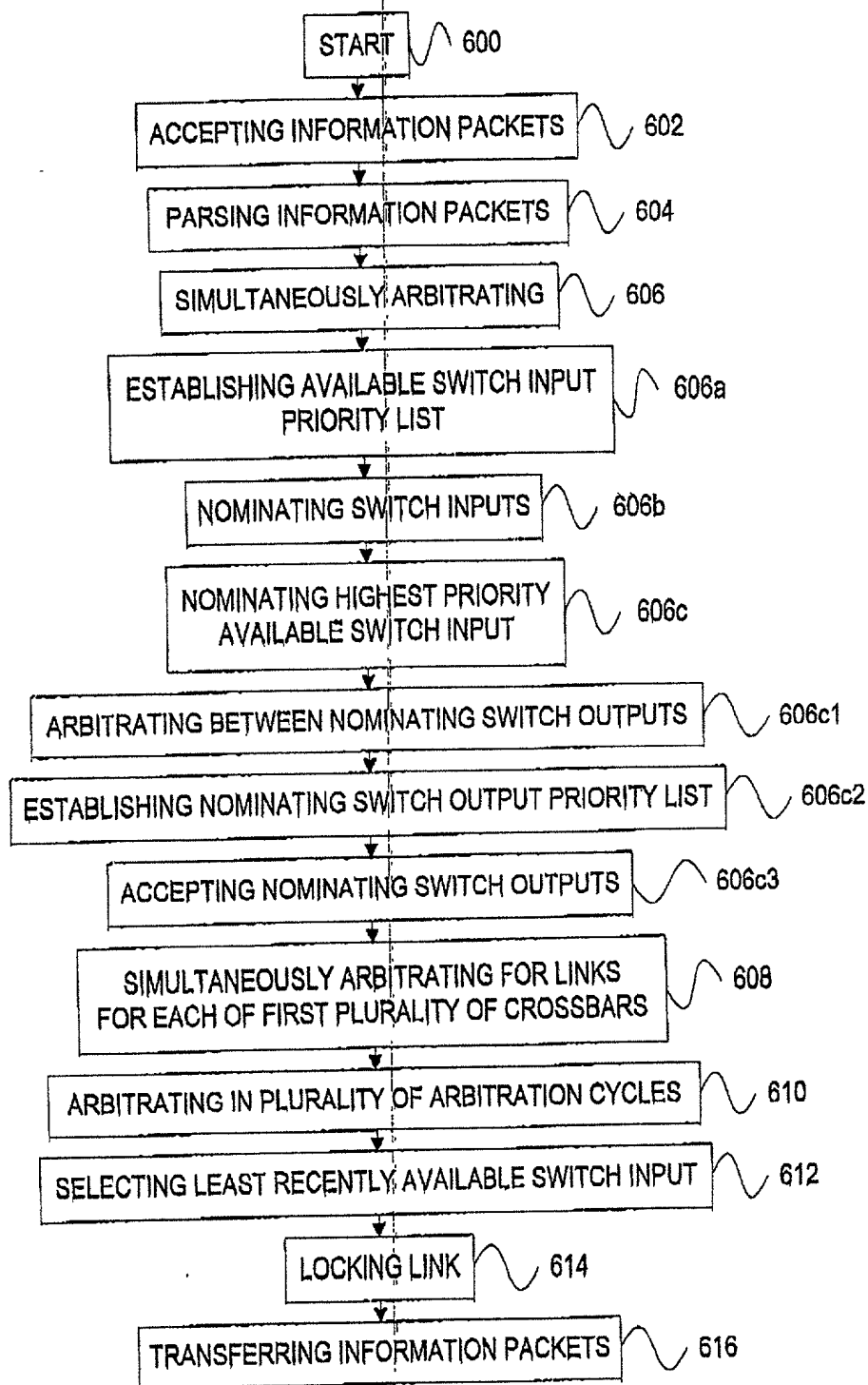


FIG. 6

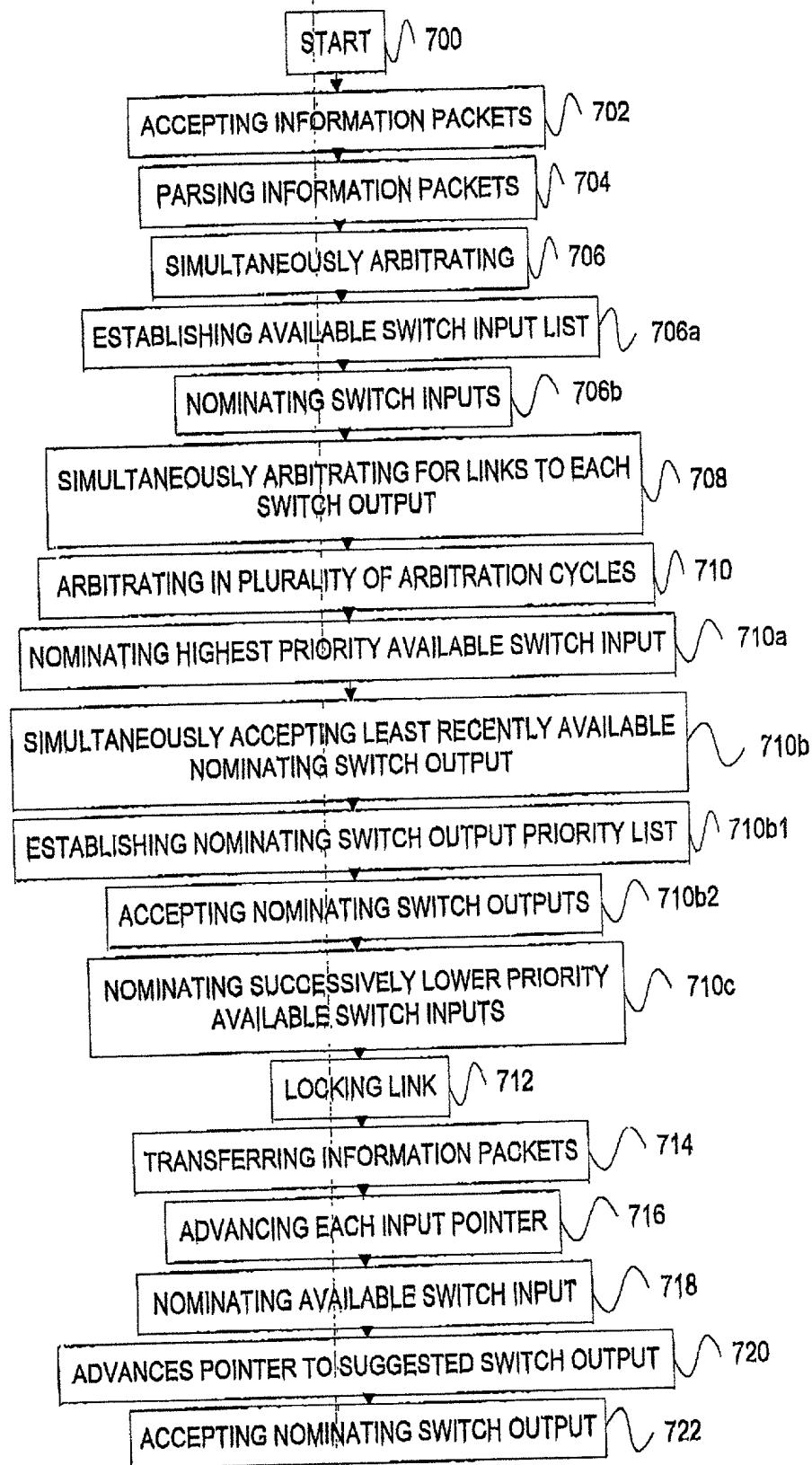


FIG. 7

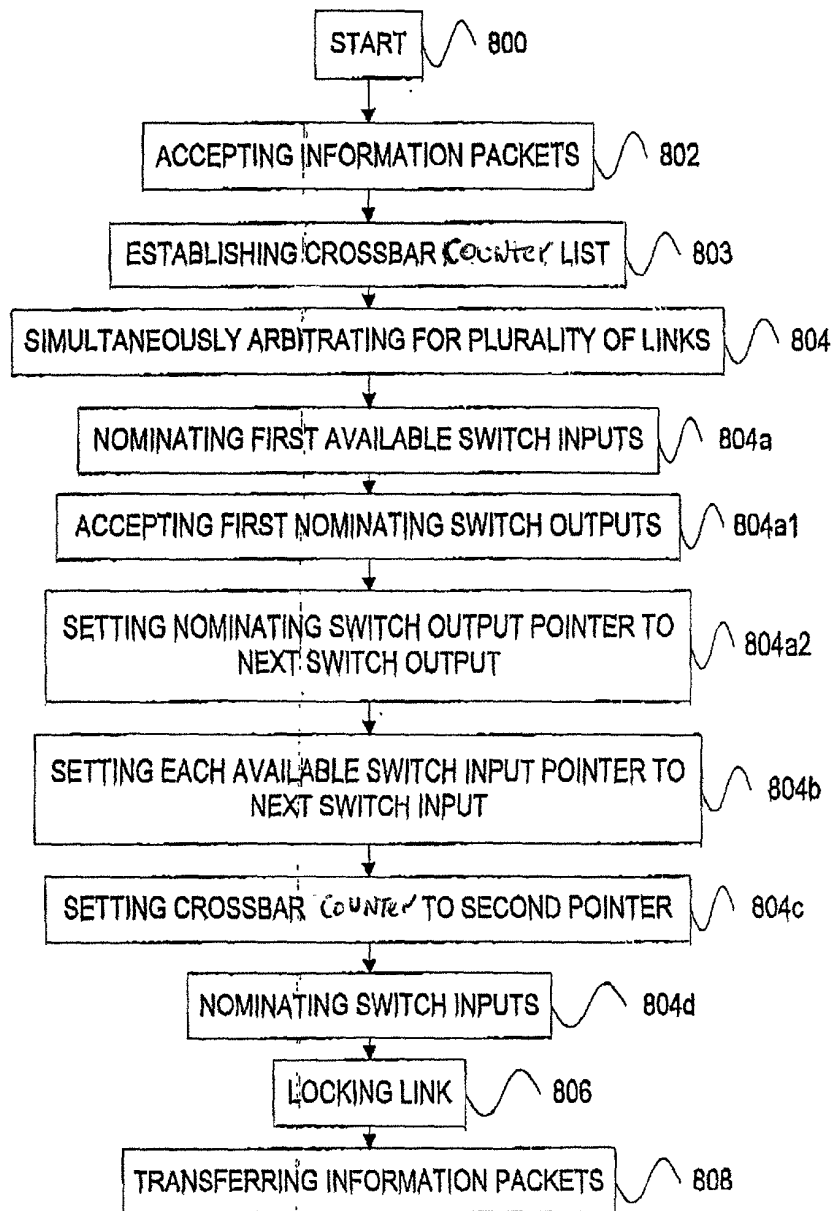


FIG. 8

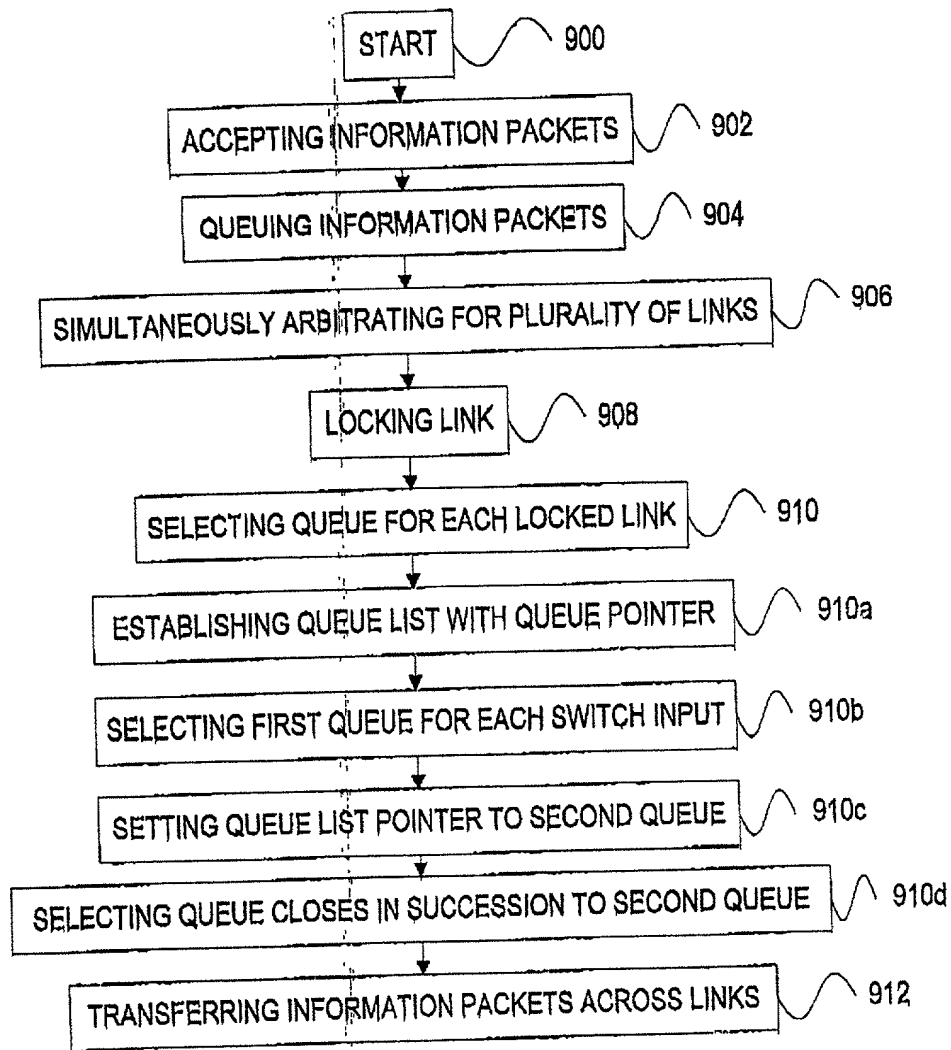


FIG. 9

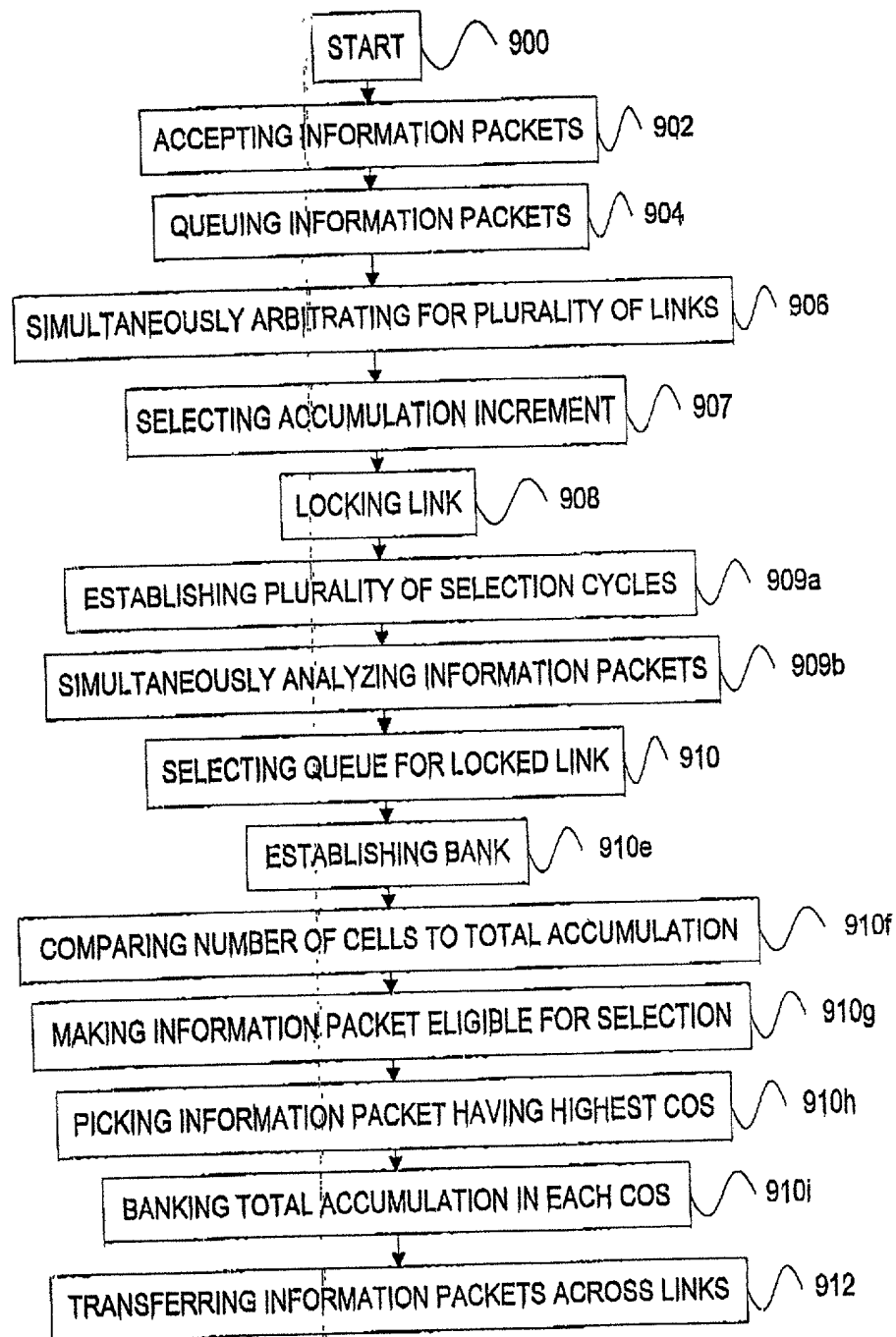


FIG. 10

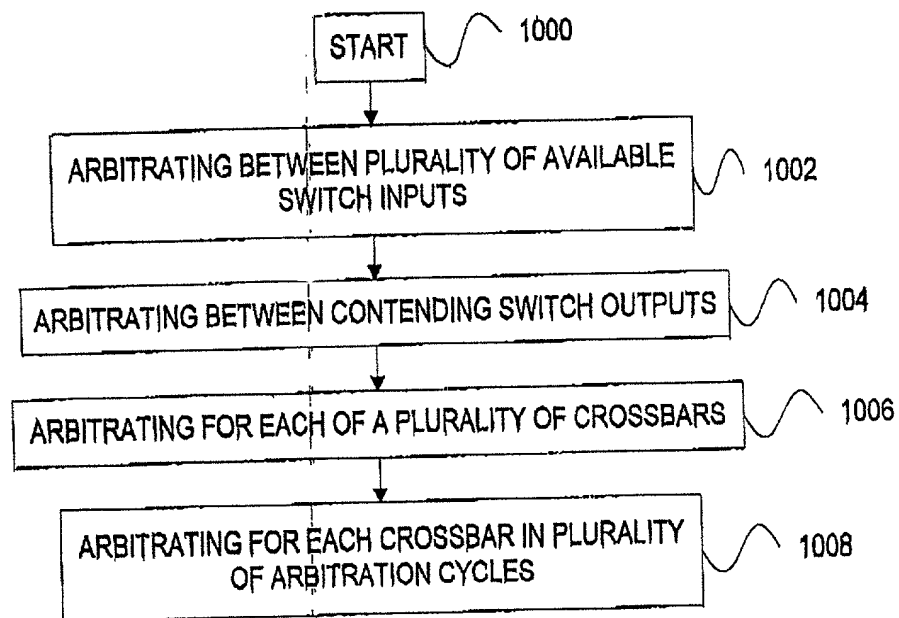


FIG. 1